

Day : Friday Date: 5/22/2009

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Inventor Name Search Result

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ALL INVENTORS SEARCHED, KD 5/22/09

| Application# | Patent# | PG Pub# | Status | Date Filed | Title | Examiner Name |
|--------------|---------------|---------|--------|------------|--|---------------|
| 06126663 | 4630795 | | 150 | 03/03/1980 | SUSPENDABLE DISPLAY RECEPTACLE | FOSS,J |
| 06620084 | 4605191 | | 150 | | SUSPENDABLE DISPLAY RECEPTACLE | FOSS,J |
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| 06634552 | 4601453 | | 150 | 07/26/1984 | OPEN REEL ADJUSTABLE HANGER | FOSS,J |
| 07264705 | Not Issued | | 161 | 10/31/1988 | TEMPLATE FOR FASTENING A CONTAINER TO A SURFACE | NOT,DEFINED |
| 07775161 | 5301298 | | 150 | 10/11/1991 | PROCESSOR FOR MULTIPLE CACHE COHERENT PROTOCOLS | NGUYEN,HIEP |
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| 07777763 | Not Issued | | 166 | 10/11/1991 | PROCESSOR CACHE MEMORY WHERE BOTH PHYSICAL AND VIRTUAL TAGS ARE STORED | LANE,JOHN |
| 07777765 | 5379396 | | 150 | 10/11/1991 | WRITE ORDERING FOR MICROPROCESSOR DEPENDING ON CACHE HIT AND WRITE BUFFER | TALL,MICHAEL |

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| 08195827 | Not Issued | 166 | 02/10/1994 | VERSATILE CACHE MEMORY | LANE,JOHN |
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| 08265495 | 5574872 | 150 | 06/23/1994 | METHOD AND APPARATUS FOR CONTROLLING THE SAVING PIPELINES IN PIPELINED PROCESSORS DURING TRAP HANDLING | HARRELL,ROBEF |
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| 08438615 | 5717898 | 150 | 05/10/1995 | CACHE COHERENCY MECHANISM FOR MULTIPROCESSOR COMPUTER SYSTEMS | LANE,JOHN |
| 08634638 | Not Issued | 161 | 04/18/1996 | PHYSICAL ADDRESS SIZE SELE©TION AND PAŒE SIZE SELECTION IN AN ADDRESS TRANSLATER | BRAGDON,REGIN |
| 08978654 | 5922378 | 150 | 11/26/1997 | WATER FILTRATION VESSEL | WEIER,ANTHON' |
| 09418591 | 6373786 | 150 | | CAP FOR A HERMETICALLY SEALED CONTAINER | ROSKOSKI,BERN |
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| 10052435 | Not Issued | 20020150106 | 61 | | Handling multiple network transport service levels with | MADAMBA,GLEN |

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